EE 330
Homework 2
Fall 2022

Due Friday Sept 2 at noon

On this and subsequent HW assignments there will be problems that require a Verilog or VHDL solution. It will be assumed that students either have a background in Verilog or VHDL or that they will study what is needed to develop this background. There are numerous sources of material on Hardware Description Languages available online. The text for the course also has a short discussion on HDL in Sec. 1.8 and a more extensive discussion in Appendix A.

## Problem 1 (10 pts)

What is the purpose of the DRC and LVS steps in the Cadence design flow?

## Problem 2 (10 pts)

The cost per good die is $3 and the die come from a wafer that is a 45cm diameter wafer which costs $3000 per wafer. The die size is 0.5 $cm^2$. What is the yield of the die? (neglect die loss on the edges of the wafer)

## Problem 3 (10 pts)

Assume a 300mm wafers cost $3200. If the defect density on this wafer is 1.5/cm$^2$, determine the cost per good die if the die is square with a side dimension of 6 mm. Assume the soft yield is 100%.

## Problem 4 (10 pts)

Determine the soft yield of a device that has a current bias requirement of 1mA to 3mA if the current bias has a Gaussian distribution with a standard deviation of 0.17mA and a mean of 2mA. How does the soft yield change if the mean is 1.5mA?

## Problem 5 (10 pts)

Assume a particular function in a $14nm$ process being used today requires a die area of $0.25cm^2$ and that it is fabricated on $300mm$ wafers. Predictions suggest that in a few years, high-end processes will have $3nm$ feature sizes on $450mm$ wafers. Assuming the circuit schematic does not change but the transistor sizes scale with feature size, how large will the die area be on the new, $3nm$ process? How many will you be able to fit on the $450mm$ wafer when waste due to wafer edge and saw lanes are neglected?

## Problem 6 (10 pts)

Assume you are an engineer working on IC fabrication for a large semiconductor company. You are told that a new circuit for a Delta-Sigma ADC is in the works and that its die is anticipated to have an area of $0.85mm^2$. You also know that wafers processed at your fab house tend to have a defect density of $1cm^{-2}$ and the chip has a predicted soft yield of 99%.

a) What is the hard yield of the die?
b) What is the overall yield?
c) Assume that the semiconductor company has a policy of not fabricating die that have a kyield that is lower than 95% . As specified, is the ADC suitable to be produced in the fab? If so, how much larger could the designers let the die area be before falling below the 95% yield limit? If not, how low of a defect density would a fab need to be able to achieve the 95% yield?

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## Problem 7 (10 pts)

Assume the specified offset voltage for each of the 2 amplifiers in a "dual" op amp is 5mV (that is, $|V_{OS}|<5mV$). Determine the soft yield for the "dual" op amp integrated circuit (i.e. both op amps must meet the $V_{OS}$ specification) if the standard deviation of the offset voltage for each op amp is 3 mV and the mean is 0V. Assume the offset voltage for each of the 2 amplifiers are uncorrelated and that the distribution of the offset voltages are Gaussian.

## Problem 8 (20 pts)

Using ModelSim create a 4-input **NOR** and a 3-input NAND gate. Create a test bench for the code to verify the operation of the design. Provide both your code and the test bench results (appropriate results/waveforms). Use the same input signals for verifying the operation of the **AND** and **NOR** gates in the test bench.

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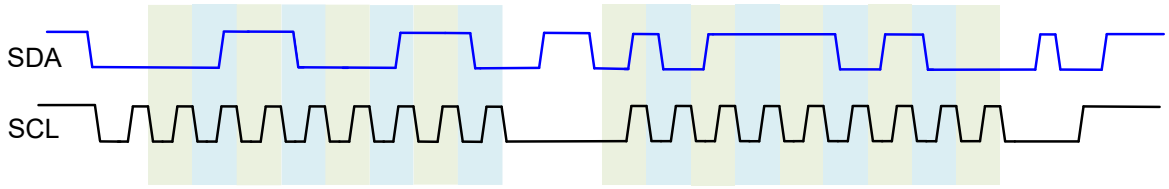
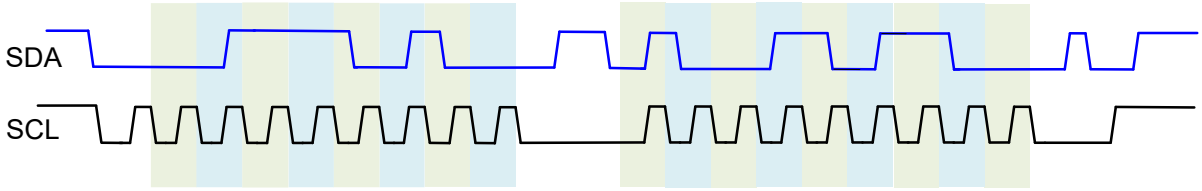
Circuit designers are often expected to understand a customer's or clients problem as well or better than the client to design an integrated circuit that will meet the needs of the customer. One common application on many systems is a serial or parallel digital communication protocol. There are numerous standard protocols for communications. The following problem focuses on understanding one of these standard protocols. You may need to seek outside sources for some information about the protocols. It has been included as an extra credit problem rather than a required problem since we have a short week for this assignment but it should be a good learning experience.

## Problem 9 (Extra Credit 20 pts)

There are several different protocols used for communicating between devices on a chip, between chips on a PCB, or between different systems. Some are serial and some are parallel. Included in the communication protocols are SPI, UART, USB, and $I^2C$. This problem will focus on $I^2C$. $I^2C$ is a 2-wire (plus ground) open-drain protocol where one or more devices are designated as a Master and the remaining devices are designated as slaves. The 2 wires connecting the devices can be referred to as an $I^2C$ bus. With this protocol, communications ports of the devices are placed in parallel on the 2-wire bus. The two nodes in the $I^2C$ bus are designated as SDA and SCL. In standard $I^2C$ protocol there can be up to 128 slave devices each with unique addresses of <A6,A5,A4,A3,A2,A1,A0>. Assume in a system with a single Master, the following two data sequences on these two nodes were obtained (shading has been added to better visualize the relationship between SDA and SCL) where high levels on both nodes are 1.2V and low values are 0V.




Data Sequence 1




Data Sequence 2

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a) Describe what Data Sequence 1 represents
b) Describe what Data Sequence 2 represents
c) What does the term “open-drain” mean?
d) The $I^2C$ protocol is noted for not having logic contention. What does this mean?
e) Why can devices with modestly different logic levels coexist on the same $I^2C$ bus?